

1 Introduction

The user guide provides guidelines on how to help you successfully design the HME-M7 board which includes the power supply, configuration, clock, DDR2 or DDR3, high speed USB, LVDS and ADC schematic and PCB layout guidelines.

This document provides guidelines for the hardware board design schematics that incorporate HME-M7 FPGAs. Good board design practices are required to achieve the expected performance from the printed circuit board (PCB) and HME-M7 devices. High quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements, and using appropriate transceiver protocols. These guidelines should be treated as a supplement to standard board-level design practices. This document assumes that the reader has a good understanding of the HME-M7 chip, is experienced in digital and analog board design, and knowledgeable in the electrical characteristics of systems.

2 Power Supply

HME-M7 devices power supplies are majorly classified as:

- Core power supply
- I/O power supply
- USB power supply
- Double data rate (DDR) power supply
- Phase-locked loop (PLL) power supply
- ADC power supply

Table 1 Power Supply

Symbol	Parameter	Min	Typ	Max
VDD_CORE	Core power	0.9V	1.0V	1.1V
VDD33	JTAG/FLASH power	2.97V	3.3V	3.63V
VCC33A_PLL	USB PHY PLL power	2.97V	3.3V	3.63V
VCC33A_HSRT	USB PHY power	2.97V	3.3V	3.63V
RTC_VDDBAT	RTC Power		2.0	
VDDADC	ADC Power	2.97V	3.3V	3.63V
VDDIO	I/O supply voltage @ 3.3V	2.97V	3.3V	3.63V

Symbol	Parameter	Min	Typ	Max
	I/O supply voltage @ 2.5V	2.375V	2.5V	2.625V
	I/O supply voltage @ 1.8V	1.71V	1.8V	1.89V
	I/O supply voltage @1.5V	1.425V	1.5V	1.575V

Note:

The VDD33 voltage can be 1.5/1.8/2.5/3.3V if HME-M7 is used as PS mode.

2.1 Power Supply Sequencing

The HME-M7 devices start to work when the VDDCORE and VDD33 reach their trigger point.

trigger point:

- VDDCORE: 0.7V
- VDD33: 1.86V

The VDDCORE must reach the trigger point voltage before the VDD33.

The rising time range of VDDCORE and VDDIO is from 200ns to 1s

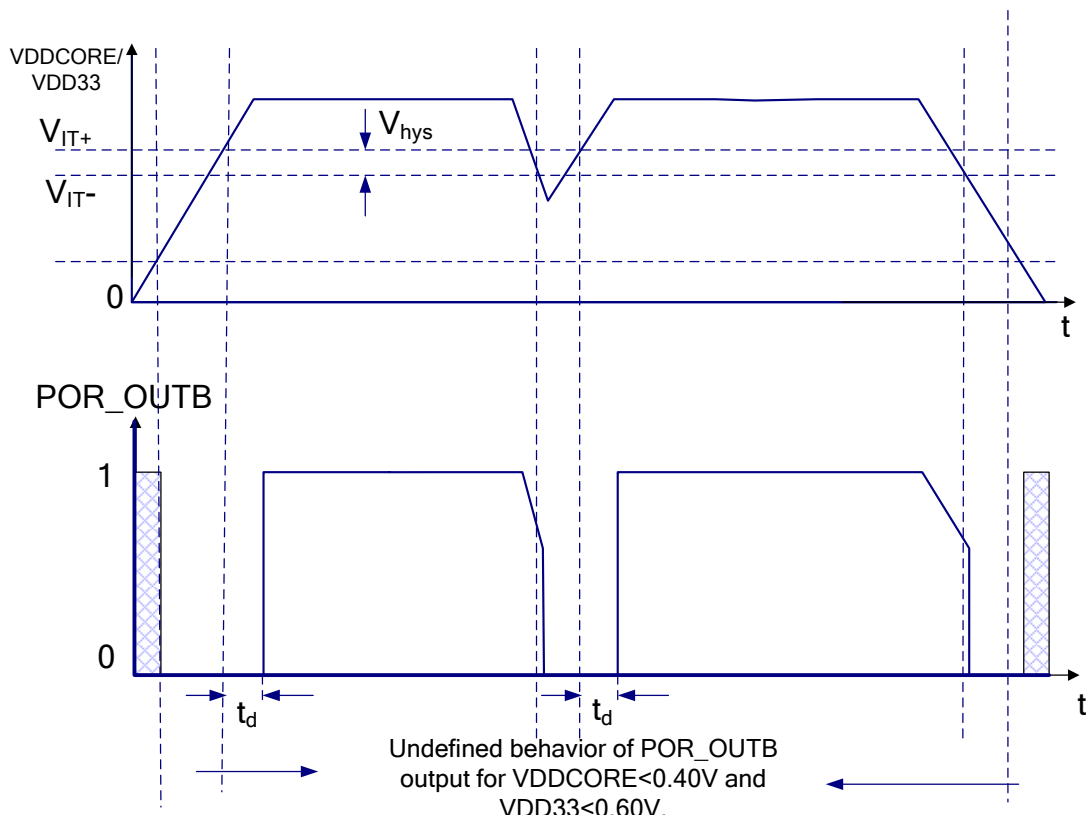


Figure 1 POR waveform

2.2 Power Supply Decoupling

2.3 Core Supply

The core power supply must have low noise and low ripple voltages per datasheet. Proper care should be taken while designing the power supply (V_{DD_CORE}) for core. Proper placement of decoupling caps and plane geometry greatly influences the power supply distribution going into HME-M7 devices.

2.3.1 Component Placement

- The bulk capacitors (330 uF or 100 uF) should be placed near by the HME-M7 device.
- The bypass capacitors (47 uF and 22 uF) should be placed near, or if possible, on the periphery of the device.
- All decoupling capacitors (0.1 uF and 0.01 uF) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of ball grid array (BGA) package pins. These decoupling capacitors are carefully selected to have low impedance over operating frequency and temperature range. Capacitor pad to via trace should be as small as possible. HME recommends keeping the capacitor pad directly on the corresponding vias. The capacitors should not share ground vias. Each decoupling capacitor should have its own via connection to PCB ground plane.

2.3.2 Plane Layout

- HME recommends using the V_{DD_CORE} plane as shown in Figure 2.

Note: There are many ways the plane can be routed. The goal is to have a dedicated and low impedance plane.

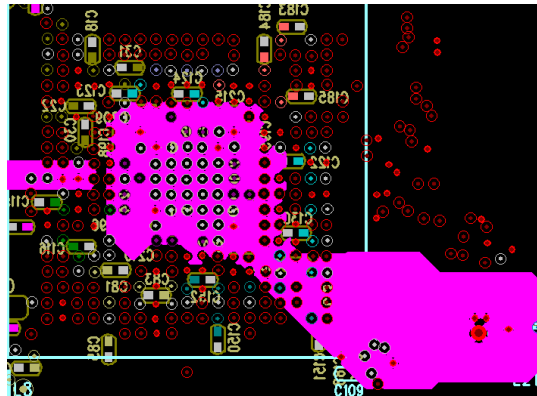


Figure 2 POR waveform

3 LVDS

The bank 3/4 and bank11/12 of HME-M7 have LVDS I/O, so the VDDIO must be 2.5V if they are used as LVDS.

The fast edge rate of an LVDS driver means that impedance matching is very important – even for short runs. Matching the differential impedance is important. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the canceling magnetic field effect of differential lines and will be radiated as EMI.

Controlled differential impedance traces should be used as soon as possible after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12 mm or 0.5 in. Also, avoid 90° turns since this causes impedance discontinuities; use 45° turns, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs that appear and radiate as common mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias to minimize inductance to the power planes.

4 Differential traces

LVDS utilizes a differential transmission scheme, which means that every LVDS signal uses two lines. The voltage difference between these two lines defines the value of the LVDS signal. For successful transmission of LVDS signals over differential traces, the following guidelines should be followed while laying out the board.

- **Use controlled impedance PCB traces that match the differential impedance of your transmission medium (e.g., cable) and termination resistor. Route the**

differential pair traces as close together as possible and as soon as they leave the IC. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

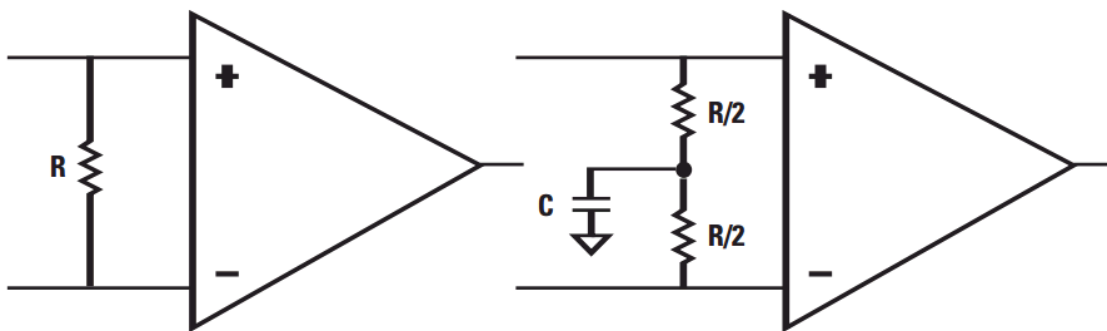
- Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair will result in a phase difference between the signals. That phase difference will destroy the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/\epsilon_r$ where c (the speed of light) = 0.2997 mm/ps or 0.0118 in./ps). A general rule is to match lengths of the pair to within 100 mils.
- Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to ensure isolation between pairs of differential lines.
- Minimize the number of vias and other discontinuities on the line.
- Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.
- Within a pair of traces, the distance between the two traces should be minimized to maintain common mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to “imbalances” is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. For the best results, both lines of the pair should be as identical as possible.

5 Termination

HME-M7 LVDS differential pairs have the internal termination resistor whose range is about from 60 to 120 Ω . You can use internal termination which can be set by Primace IO editor or external termination resistor.

- Use a termination resistor that best matches the differential impedance of your transmission line. It should be between 90 Ω and 130 Ω for point-to-point cable applications. Remember that the current mode outputs need the termination resistor to generate the proper differential voltage. LVDS is not intended to work without a termination resistor.
- Typically, as in figure, passive resistor across the pair at the receiver end suffices.
- Surface mount resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7 mm (12 mm max.).

- Resistor tolerance of 1% or 2% is recommended. Note that from a reflection point of view, a 10% mismatch in impedance causes a 5% reflection. The closer the match, the better. Match to the nominal differential impedance of the interconnect. For ultidrop/multipoint applications, match the differential impedance to the fully loaded case.
- 5. Center tap capacitance termination may also be used in conjunction with two 50Ω resistors to filter common-mode noise at the expense of extra components if desired. This termination is not commonly used or required.



Where $R = Z_{DIFF}$ (between 100 | and 120 |), $C \oplus 50$ pF

Components should be surface-mount components, placed close to the receiver.

Figure 3 Common differential termination schemes

6 Design practices for low EMI

The two most important factors to consider when designing differential signals for low EMI are 1) close coupling between the conductors of each pair and 2) minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown in Figure 4. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors. This practice will lead to closer coupling between the conductors, as compared with the coupling between each conductor and the power/ground planes. A good rule is to keep $S < W$, $S < h$, and x greater or equal to the larger of $2S$ or $2W$. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

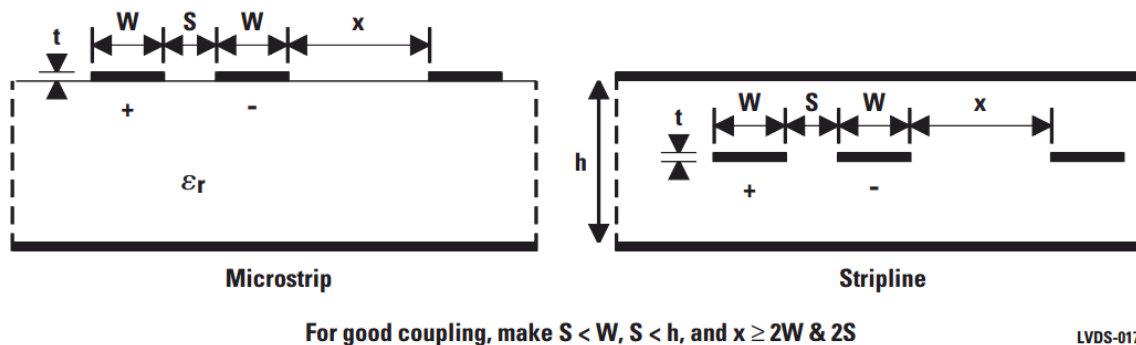


Figure 4

It is also important to minimize imbalances in order to reduce EMI. Complex interaction between objects of a system generate fields and are they are difficult to predict (especially in the dynamic case), but certain generalizations can be made. The impedance of your signal traces should be well controlled. If the impedances of two trace within a pair are different, it will lead to an imbalance. The voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

There is a basic rule to follow. Any unavoidable discontinuity introduced in proximity to differential lines should be introduced equally, to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, and PCB traces. Remember that the key word is balance.

7 LVDS Layout

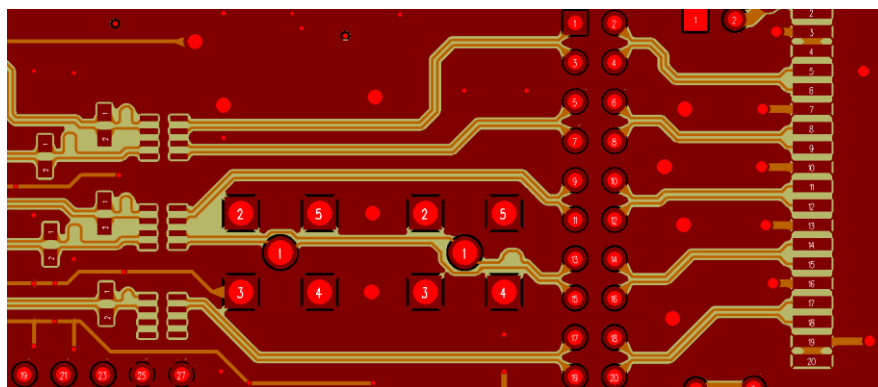


Figure 5 LVDS layout

7.1 LVDS Connectors

Connectors can be used to connect the LVDS signals from one board to another.

Figure 8 shows good and bad examples of the LVDS connectors. In the right example,

the differential pairs are the same length; in the left example, signals of the same differential pair have different lengths, thereby causing skew.

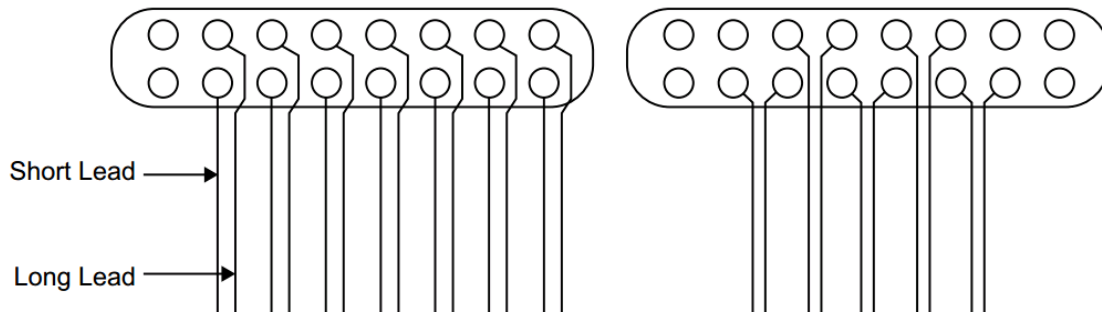


Figure 6 LVDS connector layout

Use the following guidelines while selecting connectors to be used for LVDS applications.

- **Connectors must have low skew with matched impedance.**
- **Connectors with same length leads should be selected for lower skew and crosstalk.**
- **The two members of the same differential pair must be placed adjacent to each other on the connector.**
- **Ground pins should be placed between differential pairs.**
- **End pins of the connectors should preferably be grounded and must not be used for high-speed signals.**
- **All the unused pins of the connector should be properly terminated.**

8 DDR

During the design of the DDR2 must be continuous, constant single-ended walk line impedance matching 50 Ohms resistance must be used on the all single-ended signal and to achieve the impedance matching, and for the differential signal, terminal impedance matching of 100 Ohms resistor must be used all the terminal differential signal. In the design of DDR3, single-ended signal terminal matching between 40 and 60 Ohms resistance can be selected and the impedance matching resistance difference signals are always in 100 Ohms.

For DDR2 and DDR3, including signal DQ, DM and DQS are point-to-point connection way, don't need any topology, for DDR3, these all topologies are applicable, but premise condition is go line should be as short as possible. Fly - By topological structure in terms of dealing with noise, has the very good waveform integrity.

8.1 Schematic

The HME-M7 DDR I/Os have the internal termination resistors which can be configured in the Primace IO editor, so you can use the external termination resistors or not. The VTT is not required if the internal termination resistors are used.

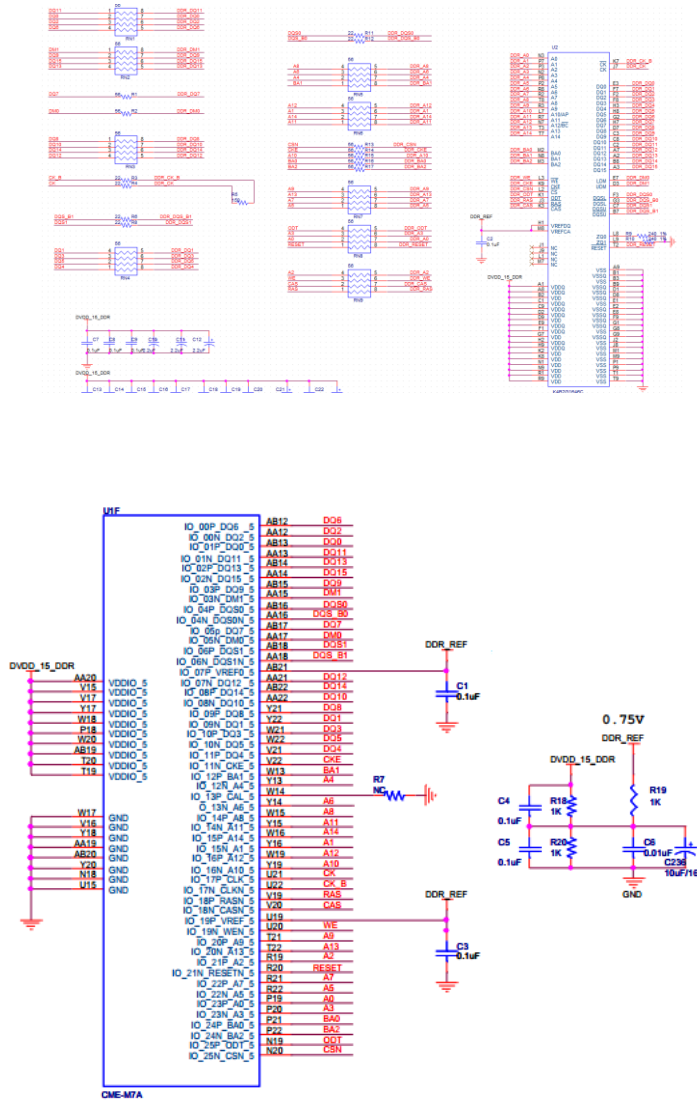


Figure 7 DDR Schematic

9 Layout Guidelines

To ensure high quality signal integrity and also to comply the high intensity of the BGA package, it is recommended to use 6-layer PCB with the following stack:

- Layer 1 : Top signal Layer
- Layer 2: Gnd Plane Layer

- **Layer3: signal Layer**
- **Layer4: signal Layer**
- **Layer 5: Power Plane Layer**
- **Layer 6: Bottom Signal Layer**

9.1.1 Power supply recommendation

An important point to take into consideration when designing such system is to guarantee that both the HME-M7 and the DDR/2/3 devices have very clean digital power supplies.

To decouple the HME-M7 requires more decouple capacitors. It is recommended that more 100nF ceramic capacitors and 10uF tantalum capacitors are distributed over the power supply pins include VDDIO, CORE power.

9.1.2 Memory bus layout general consideration

The DDR2/3 memory interface can be split three groups:

- **the data bus and its associated strobe DQ and DQS.**
- **the address bus and its associated control signals,BA0,BA1,BA2,RAS,CAS etc.**
- **the differential clock signals.**

9.1.3 Some general layout rules should be applied:

- **Maintain the integrated ground layer as a reference plane for all memory signals, that is, do not allow splits in the plane underneath both memory and HME-M7**
- **As much as possible all signals should be routed without any via between the HME-M7 and the memories. In all cases minimize the usage of vias.**
- **All ddr/2/3 traces should be as short as possible ,and traces within one group should have close length in order to reduce the skew between difference lines.**
- **All signal traces except clocks should are routed using 5/5 rules, namely 5 mil traces and 5 mils minimum spacing between adjacent traces.**
- **Clocks are routed using 5 mils traces and 8 mils spacing to 5 mils ground traces.**

9.1.4 Address bus and control signals layout

For the address bus and the control signals, a branch type net topology is recommended for better signal integrity and smaller skew than daisy chain type.

1) Data bus layout

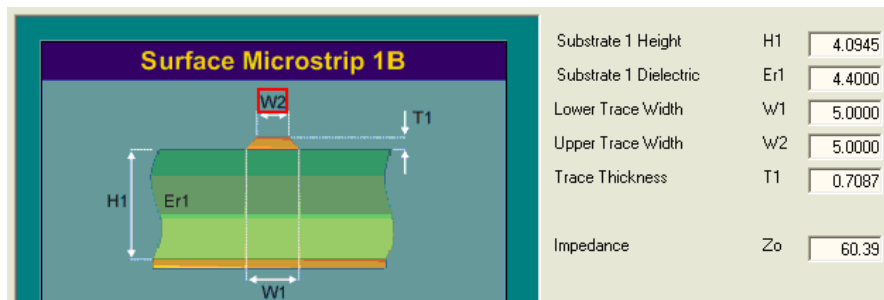
- Data lines and strobe signals within each byte group(for instance DQ[7..0],DQS0, DQS_B0) should be routed so that the maximum difference in their lengths is minimum.
- The DQS signals should have a length that is close to the longest other traces within its byte group.

2) clock signals layout

- Minimize the usage of via as much as possible.
- The clk and clk_n signals must be routed as differential signals in order to have a correct crossing point, that is, with identical lengths. The clock differential pair should be terminated by a 100ohm resistor connector between both signals, and placed close to memory chips.

3) PCB impedance calculator

- For ddr2 single signals, require 50ohm impedance matching. The figure show the result of characteristic impedance calculator (unit mil).



Delay(ps/in): D=148.467

Inductance(nH/in): L=8.966

Capacitance(pF/in): C=2.458

- For ddr2 differential clock and DQS strobes. The figure 3 show the result of characteristic impedance calculator (unit mil).

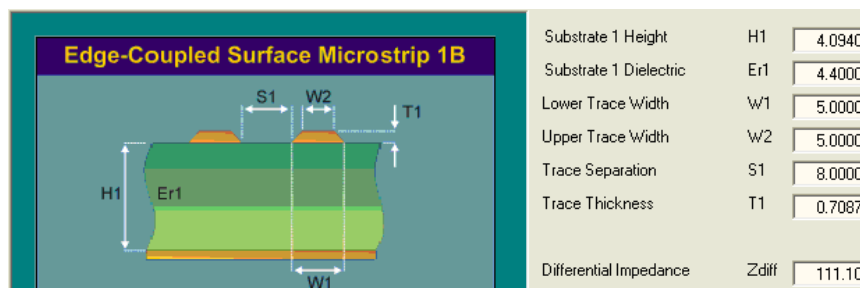


Figure 8

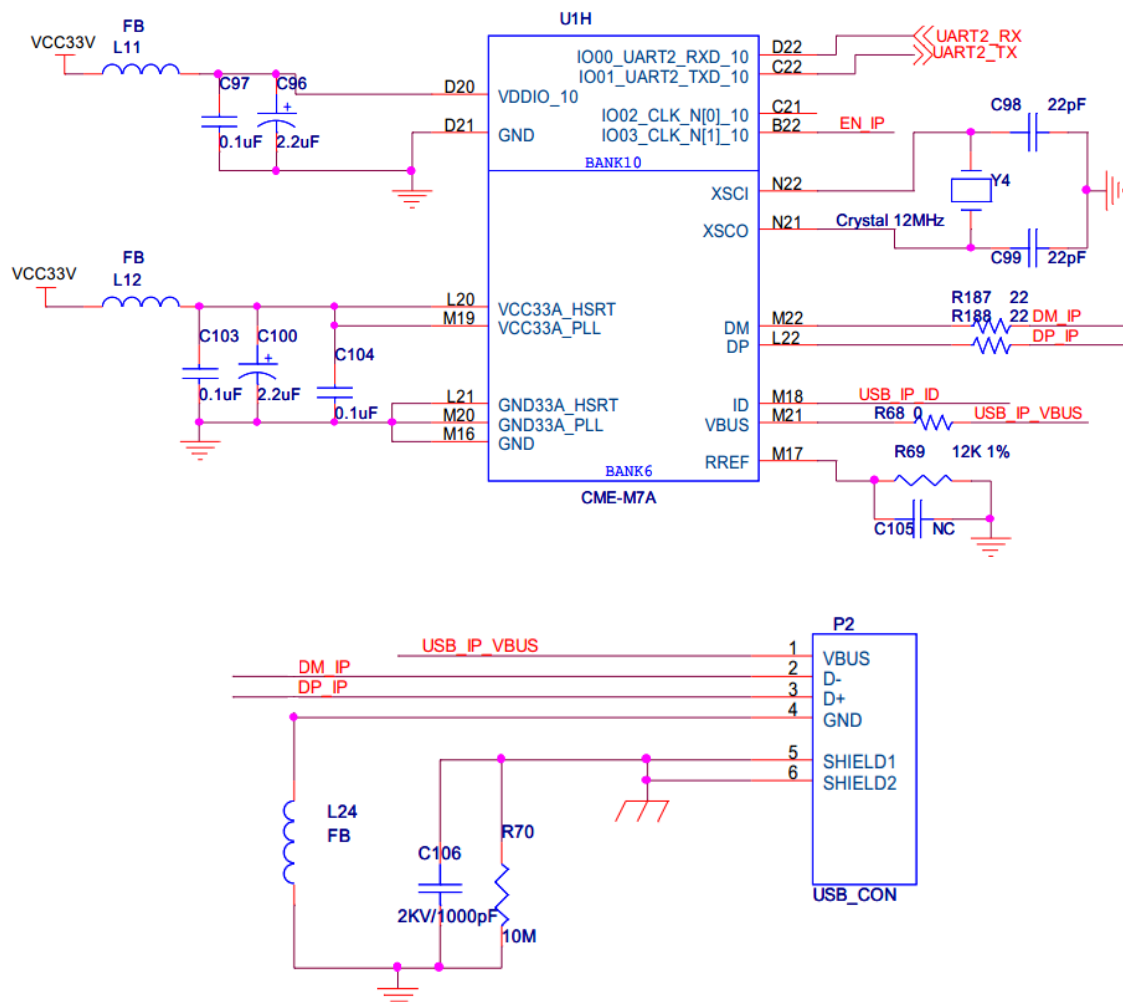
Delay(ps/in): D=142.469

Note: Application Polar Si9000 PCB Transmission Line Field Solver v6.0.0

10 USB

HME-M7 devices have an embedded USB PHY.

11 Schematic



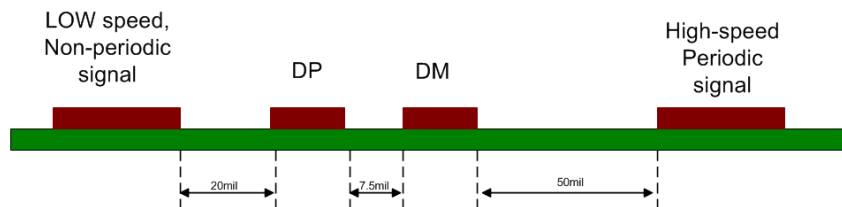
Note:

- 1). User can use the external crystal or internal clock source as USB reference clock by the `spine_usbref_sel` in the register `TOP_CKMUX_SEL0`.

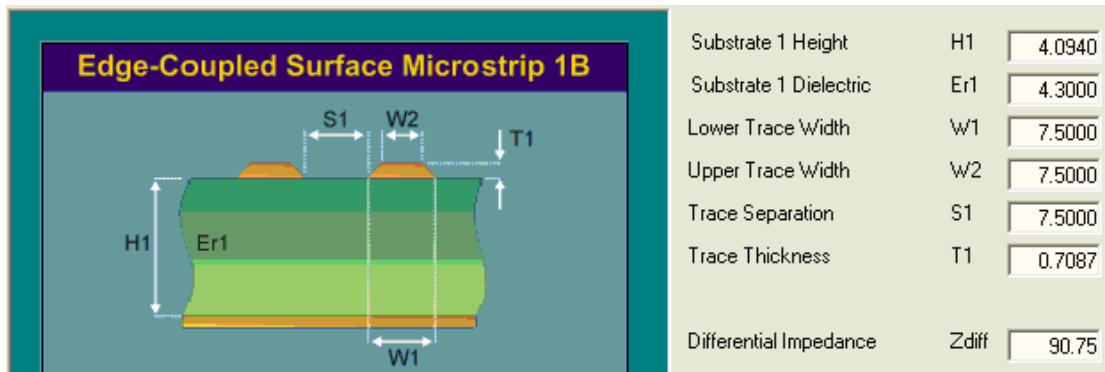
2). The DM and DP must follow the below layout guidelines

12 Layout Guidelines

- High-speed clock and periodic signal traces that run parallel to DP/DM should be at least 50 mils away from each other.
- Low-speed and non-periodic signal traces should be at least 20 mils away from each other.
- Furthermore, there are some rules just as followed:
- For a 6-layer PCB, 7.5-mil traces with 7.5-mil spacing results in approximately 90ohm differential trace impedance for DP and DN. The figure 5 shows the rule.



- Routing should be with minimum via, no right angle, only 45 degrees (or round corners) turn with smooth edges.
- Length of DP/DM, traces should be kept at minimum as possible.
- High-speed USB signal pair traces should be trace-length matched. Max trace-length mismatch between High-speed USB signal pairs should be no greater than 150 mils.
- Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices.
- Do not place any zero ohm resistors on DP/DM lines as this would change characteristic impedance.
- Figure 6 show the result of characteristic impedance calculator (unit mil).



13 Ethernet

The HME-M7 devices support 10/100/1000M ethernet controller that has MII/GMII and MDIO interface.

The ETH_PHY_INTF_SEL_I2 must be connected to GND if the ethernet control is used.

The IO_06P_ETH_PHY_GTX_CLK_4 can output 125MHz clock which can drive the GTX_CLK.

14 ADC

The HME-M7 devices have dual 12-bit 1MSPS ADC which have 8 channels input. The special ADC_VIPP, ADC_VIPN, ADC_VINN, ADC_VINP analog inputs have a higher precision than general ADC inputs that can be used as general IO. The differential N input must be connected to GND if the channels are used as singled-ended input.

The external via the ADC_VREFP and ADC_VREFN pin or internal reference can be used for the ADC. The reference voltage is 1.0V (+/-3%) and should connect a 0.1uF~10uF capacitor.

The typical schematic is shown below.

