1 Overview

This document describes how to use the on-chip oscillator in the HME HR FPGA. The on-chip oscillator can be used as clock source and has some very flexible features to help the user save power. Fuxi provides the on-chip oscillator in the IP wizard to help the user easily add the IP to their design.

2 On-Chip Oscillator features

The on-chip oscillator supports the following features:

- **16 frequency levels for the user to select, range : 2.39MHz~131.4MHz for 3.3v IO power**
- **Frequency accuracy (for PVT): ±20%**
- **Duty cycle: 50%±5%**
- **Power-down mode and standby mode**

The on-chip oscillator supports two working mode: power down mode and standby mode. Under power down mode, all the oscillator related devices are turned off. Under standby most of the core device is turned off leaving the I/O device on. Power down mode can save more power but it takes more time to wake up from power down mode to normal working mode.

3 The usage of on-chip oscillator

3.1 On-chip oscillator primitive

The user can instantiate the oscillator in the design or add the oscillator to the design through Fuxi IP wizard. The On-chip oscillator IP uses two primitives that the IP wizard can generate. The primitives for the on-chip oscillator.

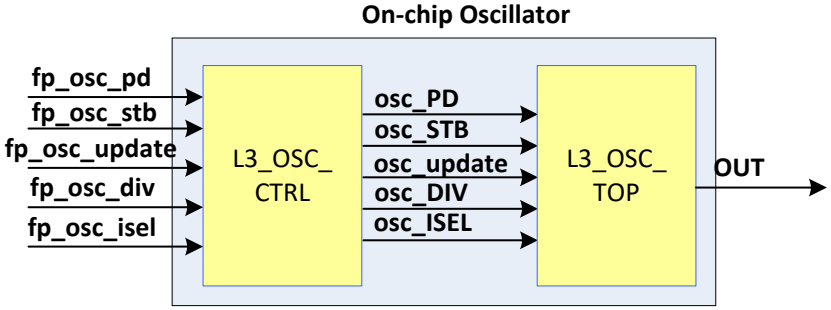

Figure 1 On-chip oscillator primitive

Table 1 On-chip oscillator primitive port description

Name	Direction	Width	Description
fp_osc_pd	Input	1	Power-down mode control 0: work normally (default) 1: oscillator power-down
fp_osc_stb	Input	1	Standby mode control 0: work normally (default) 1: standby mode
fp_osc_update	Input	1	Dynamic switch indication 0: work normally (default) 1: output frequency change
fp_osc_isel	Input	1	Charge and discharge current selection
fp_osc_div	Input	1	Output divider selection
OUT	Output	1	Oscillator clock output

Add the oscillator to the design through Fuxi IP wizard

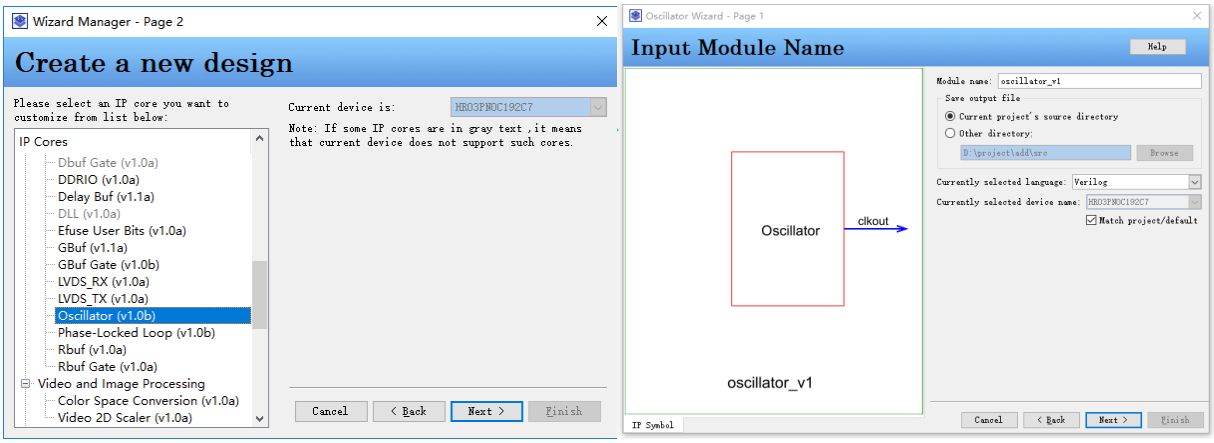

Figure 2 Add oscillator to your design through Fuxi IP wizard

Select the oscillator output frequency in the IP wizard

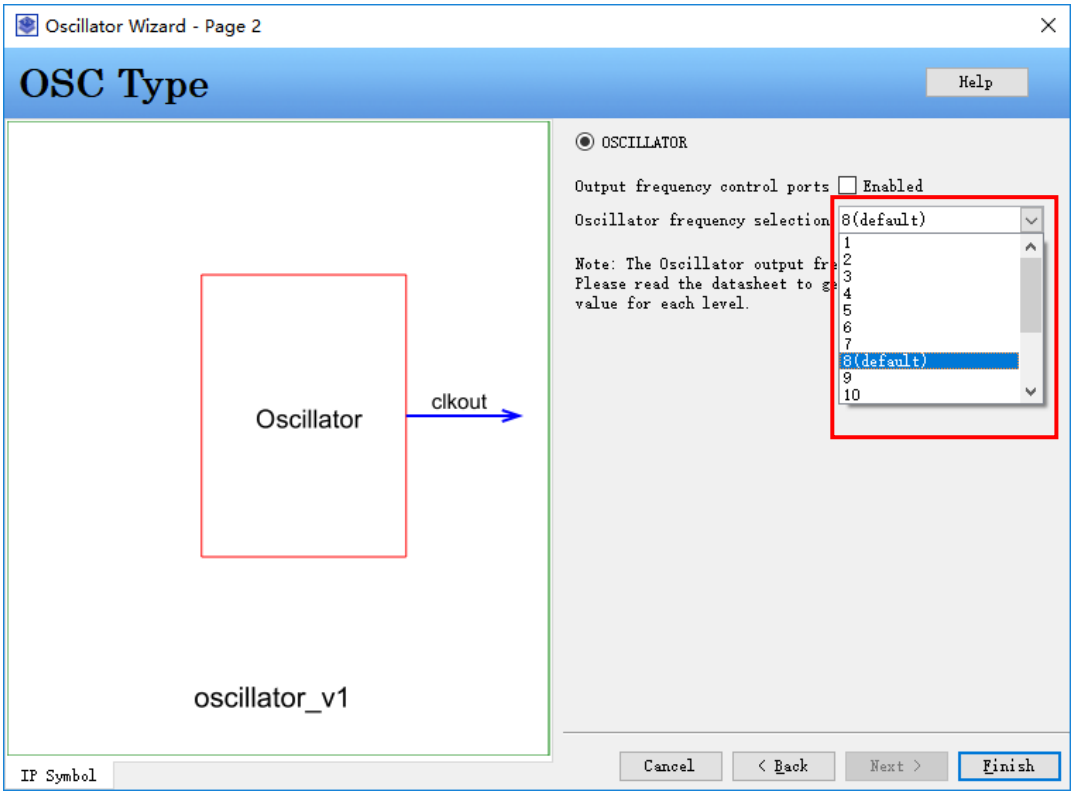

Figure 3 Select oscillator output frequency in IP wizard

The oscillator can output 16 different clock frequency, for the output frequency under different selection, please refer to **Table 2 On-chip oscillator output frequency**.

3.2 Standby and power down mode

The on-chip oscillator supports three kinds of working mode: normal working mode, standby mode and power down mode. To save power, the oscillator can be turned off by setting the oscillator into power down mode or standby mode.

The power down mode has the lowest power consumption, but will take more wake up time. The timing diagram of fp_osc_pd and fp_osc_stb is shown as below.

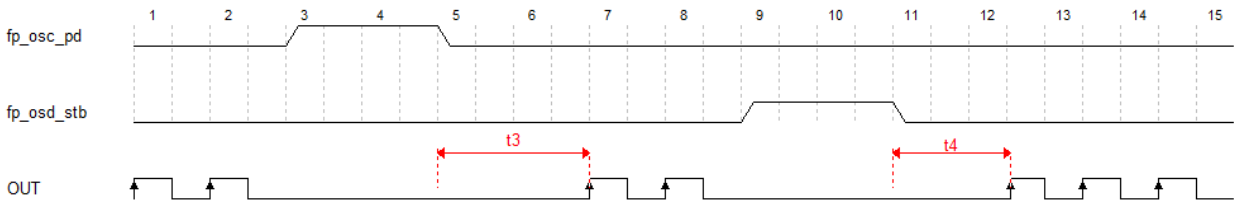

Figure 4 On-chip oscillator power down and standby mode timing

NOTE

t3<800us (wake up from power down mode), t4<800us (wake up from standby mode).

The period needed to wake up from power down mode and standby mode is different. Wake up from power down mode need more time.

By default, the on-chip oscillator is under normal working mode after POR. If user would like to save power, then the user needs to add the oscillator into their design and connect the fp_osc_pd with "1'b1".

3.3 Output frequency switching

The HR FPGA on-chip oscillator supports clock output frequency dynamic switching. User can switch the oscillator output frequency through fp_osc_isel and fp_osc_div.

The following table shows the output frequency of oscillator under different fp_osc_isel and fp_osc_div value.

Table 2 On-chip oscillator output frequency

Selection	Control				Oscillator frequencies (MHz)	
	fp_osc_isel[1]	fp_osc_isel[0]	fp_osc_div[1]	fp_osc_div[0]	For 3.3V io power	For 2.5V io power
1	0	0	1	1	**2.39**	2.30
2	0	0	1	0	**4.78**	4.60
3	0	1	1	1	**6.76**	6.52
4	0	0	0	1	**9.55**	9.20
5	1	0	1	1	**10.81**	10.43
6	0	1	1	0	**13.52**	13.03
7	1	1	1	1	**16.43**	15.88
8	0	0	0	0	**19.10 (default)**	18.39 (default)
9	1	0	1	0	**21.62**	20.86
10	0	1	0	1	**27.04**	26.06
11	1	1	1	0	**32.85**	31.75
12	1	0	0	1	**43.24**	41.72

Selection	Control				Oscillator frequencies (MHz)	
	fp_osc_isel[1]	fp_osc_isel[0]	fp_osc_div[1]	fp_osc_div[0]	For 3.3V io power	For 2.5V io power
13	0	1	0	0	**54.08**	52.13
14	1	1	0	1	**65.70**	63.50
15	1	0	0	0	**86.49**	83.45
16	1	1	0	0	**131.40**	127.00

To switch the output frequency, the fp_osc_isel and fp_osc_div must satisfy the timing requirements, the timing requirements is shown as below.

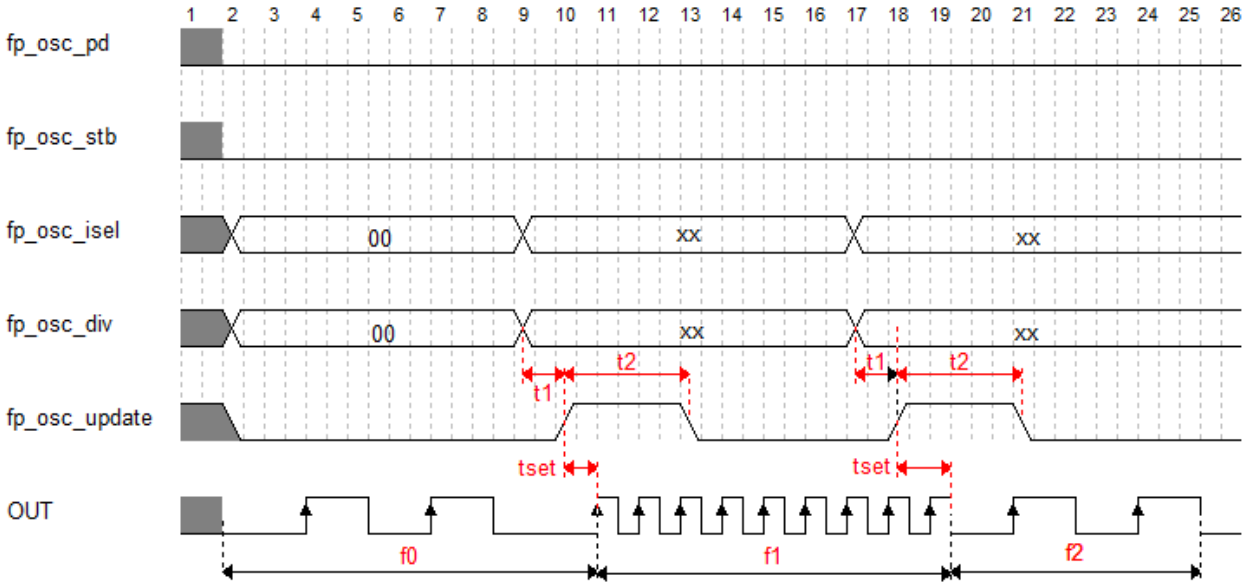

Figure 5 On-chip oscillator output frequency switching timing

Table 3 Oscillator output frequency switching timing requirements

Name	Requirements	Description
t1	>0.5ns	Assert fp_osc_update signal after fp_osc_isel and fp_osc_div has changed
t2	>1ns	The fp_osc_update signal assertion time
tset	<500ns	The setup time for output clock switching

The oscillator output-switching feature is ideal for the design with low power requirements. In typical application, specially the smart phone, wearable device application, the device needs to enter into the standby mode to save the power. In standby mode, very low speed clock is needed. Under certain

conditions, the system will be awaken from standby mode and enter into the working mode. The oscillator can be used to provide both the standby mode clock and the working mode clock without using PLL and external clock inputs. When system changes from working mode to standby mode, the oscillator switches to the low frequency clock output and when system wakes up from standby mode, the oscillator switches to the high frequency clock output.

Revision History

Date	Doc Version	Comments
Aug. 2014	V1.0	Initial release
Oct. 2018	V2.0	Update Figure2、Figure3